AMENDMENTS TO THE CLAIMS

This listing of claims supersedes all prior versions and listings of claims in this application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

a low resistance semiconductor substrate;

a high resistance semiconductor layer formed on said low resistance semiconductor substrate;

an insulation layer formed on said high resistance semiconductor layer;

a transistor element composed of a collector region, a base region, and an emitter region which are formed in said high resistance semiconductor layer;

an emitter electrode formed in said insulation layer so as to be electrically connected to said emitter region;

a sub-emitter electrode formed in said insulation layer electrically connected to said emitter electrode;

a low resistance impurity-diffusion region formed in said high resistance semiconductor layer such that said sub-emitter electrode is electrically connected to said low resistance semiconductor substrate through said low resistance impurity-diffusion region[[;]],

wherein said lower resistance impurity-diffusion region extends vertically from said insulation layer to said low resistance semiconductor substrate, and wherein the impurity is one ~~conductor~~ conductivity type;

a base electrode formed in said insulation layer so as to be electrically connected to said base region; and

a base-bonding pad formed on said insulation layer so as to be electrically connected to said base electrode,

wherein said base-bonding pad is placed on said insulation layer above said low resistance impurity-diffusion region so as to be at least partially overlapped with said low resistance impurity-diffusion region.

2. (Original) A semiconductor device as set forth in claim 1, wherein said low resistance semiconductor substrate is grounded.

3. (Original) A semiconductor device as set forth in claim 1, wherein the electrical connection between said emitter electrode and said sub-emitter electrode is established by a conducting path formed on said insulation layer, and the electrical connection between said base electrode and said base-bonding pad is established by a conducting path formed on said insulation layer.

4. (Original) A semiconductor device as set forth in claim 1, wherein said insulation layer includes a conductive layer buried therein and electrically connected to said sub-emitter electrode, and said conductive layer is placed so as to at least partially encompass said base-bonding pad.

5. (Original) A semiconductor device as set forth in claim 4, wherein a part of said base-bonding pad is encompassed with said low resistance impurity-diffusion region, and the remaining part of said base-bonding pad is encompassed with said conductive layer.

6. (Original) A semiconductor device as set forth in claim 1, further comprising:

a first wiring pattern formed on said insulation layer;

an additional insulation layer formed between said insulation layer and both said base-bonding pad and said first wiring pattern;

a second wiring pattern formed on said additional insulation layer;

an additional emitter electrode formed in said additional insulation layer so as to be electrically connected to said emitter electrode;

an additional sub-emitter electrode formed in said additional insulation layer so as to be electrically connected to said sub-emitter electrode;

an additional base electrode formed in said additional insulation layer so as to be electrically connected to said base electrode; and

an additional base-bonding pad formed on said additional insulation layer so as to be electrically connected to said base-bonding pad.

7. (Original) A semiconductor device as set forth in claim 6, wherein said sub-emitter electrode has a grounded shield which is integrally extended therefrom between said insulation layer and said additional insulation layer, so as to encompass said base-bonding pad.

8. (Original) A semiconductor device as set forth in claim 6, wherein said second wiring pattern includes a conducting path for establishing an electrical connection between said additional emitter electrode and said additional sub-emitter electrode, and another conducting path for establishing an electrical connection between said base electrode and said base-bonding pad.

9. (Original) A semiconductor device as set forth in claim 1, wherein said low resistance semiconductor substrate exhibits a first conductivity type; said high resistance semiconductor layer includes a first high resistance epitaxial layer section formed on said low resistance semiconductor substrate and exhibiting the first conductivity type, and a second high resistance layer section formed on said first high resistance epitaxial layer and exhibiting a second conductivity type opposite to the first conductivity type; and said low resistance impurity-diffusion region includes a first low resistance impurity-diffusion region section formed in said first high resistance epitaxial layer section and exhibiting the first conductivity type, and a second low resistance impurity-diffusion region section formed in said second high resistance epitaxial layer section and exhibiting the first conductivity type.

10. (Original) A semiconductor device as set forth in claim 1, wherein said second low resistance impurity-diffusion region section is formed as a channel stopper region exhibiting the first conductivity type.

11-13. (Cancelled)